Modern PCB Design

Matching Router Technology With Design Challenges

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Agenda

- Challenges in PCB routing
- Design constraint types
- Bus path design
- Team collaboration
Interconnect Routing Challenges

- **Design constraints**
  - Too many; sometimes conflicting; limit flexibility
  - Must understand rules to know when they can be bent

- **Bus path design**
  - Parallel and serial structures

- **Emphasis on reduced design time**
  - Need for team collaboration and design reuse
Current State of PCB Design

- Many designs involve significant interactive labor
  - Interactive labor for the sake of “art” is diminishing
  - Use of automation within interactive tasks is evolving
- Auto-routers often used for place/routing strategy evals
- Designers iterate between automatic & interactive tasks
  - Auto route typically not a push-button solution
- High volume of design constraints demand a high level of creativity from designers
- Engineering and layout designer roles are blending
- The traditional “one layout, one designer” methodology is being challenged
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Current State of Constraints

- Designers want manual-like results that meet constraints
  - Want tools that follow placement/routing concepts in their head
- More constraints are used to get the tool to follow designer intent
- Too many constraints cause the router to fail
- Need to abstract constraints so router will succeed
- Constraints transfer intent to others for multiple shifts, ECOs
Design Constraint Types

- Electrical
- Manufacturing
- Mechanical
- Thermal
- Reliability
- ...

[Images of circuit designs and constraints]
Electrical Constraints

**Timing**

- Constraints specified as length or delay
  - Individual nets or matched groups
  - Must also assign net topologies
  - Pin-to-pin (real or virtual) constraints
- After part placement, the only timing control available is lengthening
- Tuning can introduce additional problems
Electrical Constraints

**Crosstalk**

- Constraints specified as crosstalk (mV) or parallelism (length/spacing tables)
  - Crosstalk value is more accurate but requires definition of additional driver data
- Crosstalk tuning is usually done after most routes are complete
Electrical Constraints

**Differential Pairs**

- Constraints include
  - Pair tolerance
  - Convergence length
  - Separation length
  - Differential spacing
- Must ensure topologies match
- Route, then tune to delay
Manufacturing Constraints

*Design for Fabrication*

- Standard clearances
  - Trace, pad, via, plane
  - By net class and by layer
- Acid traps
- Embedded passives
- Cavities
- Lead-free materials
- Materials and stack-up dependent on target fabricator
Manufacturing Constraints

*Design for Assembly*

- Component type clearances
- Target assembly equipment
- Lead-free soldering processes
- Reflow or wave solder
- Rework requirements
- Bare die: wire bonds, die stacking
Manufacturing Constraints

Design for Test

- Test point placement
  - Impact of via-in-pad and BGA fanouts
- Make sure access points available during fanout
- Collaborate with engineer regarding % coverage
- Define test point regions relative to neighboring parts
- Test methodology dependent on operating frequency
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Differential Pairs and Multi-Gigabit

- Synchronously clocked “parallel” architectures (primarily single-ended)
- Asynchronously clocked “serial” architectures (primarily differential pair)
- SERDES (serializer – at driver; deserializer – at load)

Frequency

~ 10 MHz  0.5 GHz  Multi-GHz
Benefit of Moving to Serial Interconnects

- PCI-Express @ 2.5 Gb/s
- 53% board area reduction
- Decreased layer count
- Decreased component count
- Increased bandwidth

Twice the bandwidth with ½ (or less!) the number of pins

Reduced System Cost

Intel Developers Forum, Fall 2002
PCI-e Constraints

- **Timing**
  - Tightly length-match differential pairs
  - Length-match lanes within a link
  - Minimize lengths to control losses
  - Shorter lengths produce less crosstalk

- **Stack-up**
  - Use wider traces to minimize loss
  - Allow adequate spacing for crosstalk isolation

- **Layout**
  - Keep like-direction signals away from one another
  - Maintain spacing from higher-voltage aggressors
Traditional Parallel Buses Still Exist!

- Serial interconnect only make up 10-20% of designs
- Parallel structures have long been associated with the “artistry” of PCBs
  - Improved performance (matched timing & impedance)
  - Improved ECO-ability
- Serial usage
  - Above 1GHz; low power; high noise immunity; high data rates; telecom, networking, mil/aero
- Parallel usage
  - Below 500MHz; cheap; high noise margins; simpler device architecture; consumer electronics, automotive, industrial
Parallel Bus Routing

Without adequate constraints, auto routers do this

...but designers would prefer this
Parallel Bus Routing

Typical Design Process

- Design engineer
  - Typically sketches the physical bus systems and sub-systems architecture on paper
  - Specific placement and bus interconnect guidelines remain in hard copy form with little automation

- Board designer
  - Looks for potential routing patterns that flow from component to component
  - Plans ahead, knowing why a particular group of traces must route in a certain path on a specific layer
Parallel Bus Routing
The Traditional Auto-Router

- The auto-router is inherently layer biased
- The auto-router does not plan ahead like a board designer
  - One net at a time
  - Push & shove or rip-up & retry to clean-up
  - Can’t fully support designer’s vision for component placement and interconnect flow
- It's fairly easy to spot a hand-routed board over one that has been auto-routed
  - As a result, auto-routers are largely ignored
Parallel Bus Routing

Topology-Driven Design

Old methodology

Planning

New methodology

Planning

Routing
Parallel Bus Routing

Topology-Driven Design

- Topology planning represents a higher level of abstraction for design constraints
  - Simpler to specify
  - More placement planning than routing task
- Designers don’t think Manhattan/biased
  - Buses usually flow across layer bias
- Represents efficient man/machine interaction
  - Plan / route iterations
- Potential shift in user responsibilities
  - Either engineer drives layout planning…
  …or layout designer takes on engineering planning
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Collaboration Drivers

- Optimize system performance
  - Efficiently leverage unique skill sets of team
- Reduce design cycle time
  - Leverage local or globally dispersed teams for parallel / concurrent design
- Increase resource management flexibility
Layout Collaboration Methodologies

- **Outsourcing**
  - Design must be partitioned (isolated), then merged when complete

- **Expanded team**
  - Traditionally done with multiple shifts (at single location or “follow-the-sun”)
  - Can also use the partitioning model
Layout Collaboration Challenges

- Most layout designers are used to driving start to finish
  - Consistent planning and ownership
  - Undisciplined “teamwork” may actually be “redesign”
- Managing design partitioning and collisions
Evolving Collaboration

Resource Management

- True simultaneous design
  - Link designers over local or global networks
  - Dynamically display peer results
  - Automatically keep database current
  - Reduce design times proportionally with the number of designers working concurrently
  - Share design tasks and pressures across the team
  - Use any time in the design flow
    - Pre-placement, ECOs, documentation, etc.
  - Design review by specialists, management, manufacturing
Evolving Collaboration

Resource Management

- Utilize networked computing resources
  - Single designer harnessing the power of multiple CPUs to accelerate auto-routing
  - Geographically distributed computational resources
  - Evaluate multiple placement / routing strategies
  - Automated distribution process not efficient for smaller designs
Conclusion

■ Design challenges
  – Increasing and conflicting constraints for performance and manufacturing
  – Drive to reduce design time

■ Designers and their tools are evolving
  – Continued iteration between interactive & automatic tasks
  – Blending of engineering and layout designer roles
    ■ New breed of planning (design abstraction) tools emerging
  – The concept of “resource management” is changing